A 1.2v ΔΣ ADC Modulator Using 4-bit SAR Quantizer for Biomedical Applications by using 65nm CMOS Technology

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Abstract. This research focuses on enhancing Sigma-Delta ADC modulators for biomedical applications by leveraging the working principle of Successive Approximation ADC circuits. The proposed modulator includes a comparator, DAC, successive approximation register, and control circuit. The operational process begins with the sample and holds circuit-initiating conversions by sampling the input signal, and then compared with the DAC output. Using a 4-bit example, the successive approximation register refines the DAC output through iterative bit adjustments until the closest digital code approximation to the input voltage is achieved. Unlike other ADCs, the conversion time is independent of input voltage, occurring incrementally one bit at a time. The proposed enhancement aims to optimize Sigma-Delta ADC modulator performance for biomedical applications, ensuring high resolution and speed. Typical conversion speeds range from 2 to 5 MSPS, with resolutions varying from 8 to 16 bits, contributing to improved precision and efficiency in capturing and digitizing biomedical signals.

1 INTRODUCTION

This paper investigates the pivotal role of sigma-delta Analog-to-Digital Converter (ADC) modulators in enhancing cardiac biomarker monitoring within biomedical applications. Renowned for their high precision and low noise characteristics, sigma-delta modulators adeptly convert analog signals, particularly those from sensors monitoring cardiac parameters, into digital form[1]. This technique proves invaluable for capturing subtle variations in cardiac biomarkers. In the realm of cardiac monitoring, these modulators contribute significantly to the accurate digitization of signals representing crucial physiological parameters, such as heart rate and Electrocardiogram (ECG) waveforms. Their robust performance ensures the faithful representation of intricate cardiac patterns, facilitating precise analysis and detection of biomarkers associated with cardiovascular health. The modulators' inherent oversampling and noise-shaping capabilities further enhance sensitivity, enabling early detection of abnormalities and variations in biomarker levels[2]. The integration of sigma-delta ADC

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modulators in biomedical applications, particularly in cardiac monitoring, holds great promise for advancing diagnostic tools and wearable devices, ultimately improving the monitoring and management of cardiac conditions[3]. This paper provides comprehensive insights into the functionalities and benefits of sigma-delta ADC modulators, serving as a valuable resource for researchers, engineers, and healthcare professionals involved in developing innovative biomedical devices. The findings underscore the significance of this technology in advancing cardiac monitoring and pave the way for future breakthroughs in biomedical applications.

2 Executing Modulator Circuitry

The circuitry of a Sigma-Delta ADC modulator comprises several essential components that collaboratively perform the intricate process of analog-to-digital conversion. The initial stage involves an input analog section, often integrated with an anti-aliasing filter to prevent aliasing effects. Subsequently, the integrator plays a central role, in computing the difference between the input and feedback signals. The quantizer follows, discretizing the analog output into digital form, and mapping continuous voltage levels into discrete values. The modulator incorporates a feedback loop where the quantized output is fed back to create a high-order noise-shaping effect, a characteristic feature of Sigma-Delta modulation. A digital-to-analog converter (DAC) is utilized in this loop to convert the digital output back to an analog signal, which is then subtracted from the input signal. The entire process is governed by a clock generator to ensure proper synchronization and timing.

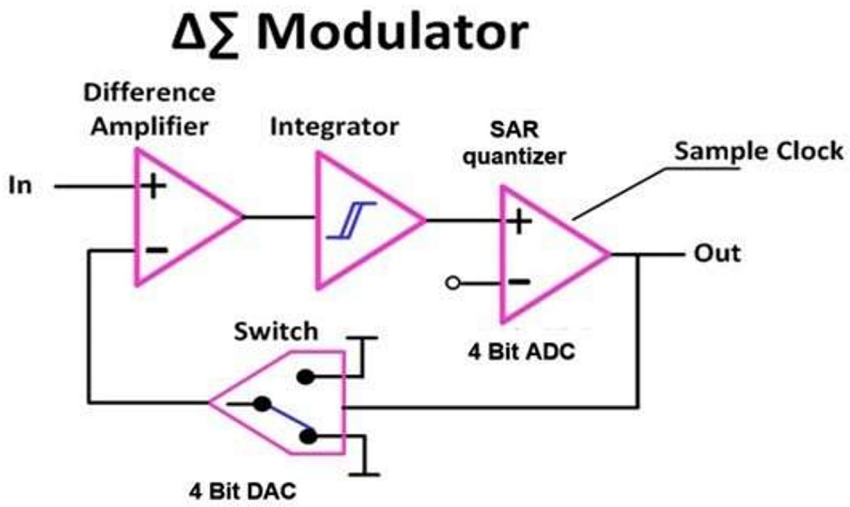

Fig. 1.4-bit sigma-Delta modulator

Further downstream, a decimation filter refines the signal in the digital domain by filtering and down-sampling high-frequency noise. The output digital stage then handles the processed signal, potentially interfacing with other digital systems or undergoing additional processing.

3 Mechanism Of Sar (Successive Approximation Register)

The Successive Approximation ADC is a fundamental circuit in analog-to-digital conversion, consisting of key components such as a comparator, a digital-to-analog converter (DAC), a successive approximation register, and a control circuit. In its operational cycle, the sample and hold circuit initiates each conversion by sampling the input signal, followed by a comparison with the DAC's output signal. Taking a 4-bit configuration as an example, the successive approximation register initially sets the most significant bit to 1 and the remaining bits to zero, establishing an initial DAC output.

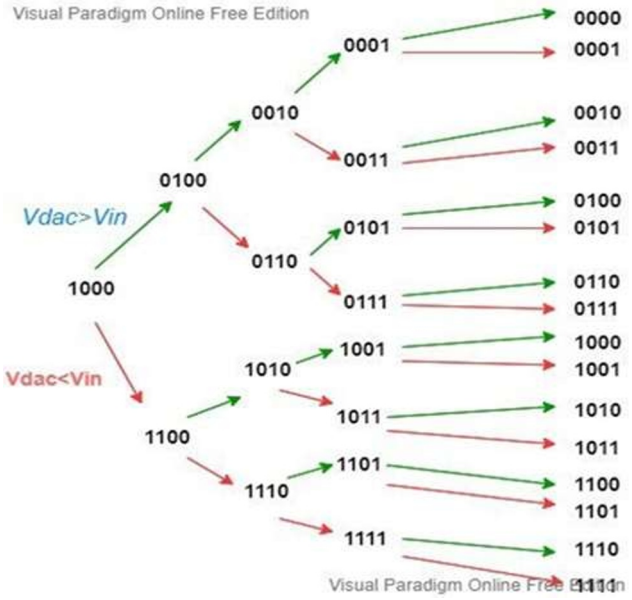

Fig. 2. Four-bit successive approximation ADC

This output is then compared to the input signal, guiding subsequent bit adjustments. The iterative process continues until the digital code representing the closest approximation to the input voltage is achieved, with the conversion occurring incrementally, altering one bit at a time through multiple iterations. The conversion time for an N-bit ADC is generally N times the clock period, and for a 4-bit ADC, it equals 4 times the clock period. Notably, unlike other ADCs, the conversion time is independent of the input voltage. These ADCs exhibit a typical conversion speed ranging from 2 to 5 Mega Samples Per Second (MSPS), and their resolution can vary from 8 to 16 bits, with some models achieving up to 20 bits. This paper delves into the detailed operational principles and performance characteristics of the Successive Approximation ADC, offering valuable insights for researchers and practitioners in the field of analog-to-digital conversion.

4 Simulation And Result

The 4-bit SAR Quantizer, operating under a reference voltage of 1V, endeavours to represent the continuous input voltage of 1.2V withindiscrete digital values. The quantization process involves a series of successive approximation steps, where the quantizeriterativelynarrows down the potential digital codes to match the input voltage.

This iterativerefinementensuresprecision in representing the analog signal with a limited bit resolution. Given the 4-bit resolution, the quantizer can generate 16 distinct digital codes (2^4). In thisspecific case, with an input voltage of 1.2V and a reference voltage of 1V, the quantizerassigns the closest digital code that best approximates the input. The output expressed in binary format, encapsulates the quantizedrepresentation of the input voltage within the limitations of the 4-bit resolution. The 4-bit output codes generated by the SAR Quantizer provide a binaryrepresentation of the quantized voltage levels. Each bit contributes to the overallprecision, with the mostsignificant bit (MSB) carrying the highestweight. A thoroughexamination of these output codes allows us to comprehend how the quantizerdiscretizes the input voltage and facilitates an evaluation of the trade-off betweenresolution and quantizationerror.

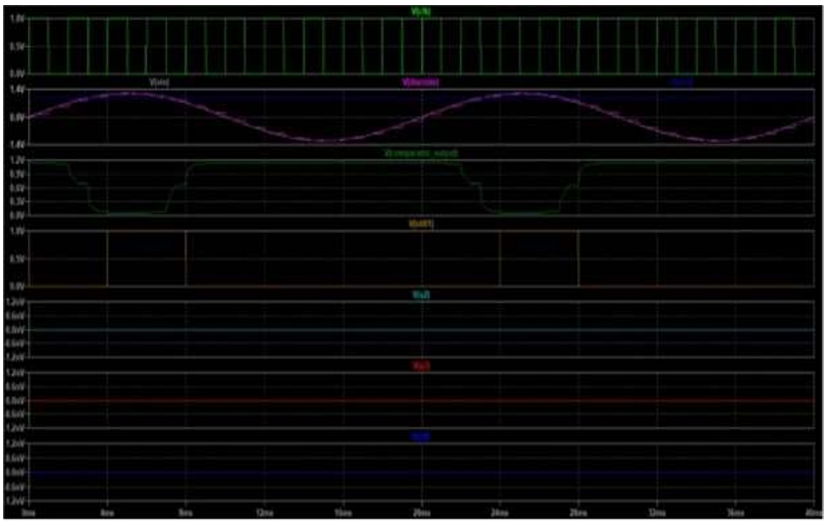

Fig. 3. Output of 4-bit SAR Quantizer

Table 2. parametersrelated to the Successive Approximation ADC

PARAMETERS	DESCRIPTION
Technology(nm)	65nm CMOS
Sampling rate (KS/s)	100MS/s
Latency(sec)	0
Input voltage(v)	1.2v
Input frequency (Hz)	50 Hz
Reference voltage(v)	1v

5 Conclusion

Successive Approximation ADC, implementedin 65 nm CMOS technology, emerges as a cornerstone in analog-to-digital conversion, boastinglow noise and zerolatency. This device'sutilization of single-cycle, low-latency-time capabilityensuresfullysettled data aftereach conversion cycle. Itsoperational cycle exemplifiedthrough a 4-bit version, underscores a systematiciterative process whereineach conversion commences with the

sampling of the input signal. Through successive comparisonswith the DAC's output signal and subsequent bit adjustments, the ADC progressively converges towards the digital code representing the closest approximation to the input voltage. Leveraging 65 nm CMOS technologyoptimizesefficiency and performance in terms of power consumption and speed. Despitevaryingresolutionsrangingfrom 8 to 16 bits and evenreaching up to 20 bits in somemodels, the typical conversion speed remains consistent, rangingfrom 2 to 5 MSPS. This paperelucidates the operationalprinciples and performance characteristics of the Successive Approximation ADC, offeringvaluable insights for researchers and practitionersengaged in the advancement of analog-to-digital conversion technologies within the realm of 65 nm CMOS technology, emphasizingitslow noise and zero-latencyattributes**.**

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